UNIVERSITY EXAMINATIONS

EXAMINATION FOR JANUARY/APRIL 2015/2016 FOR BACHELOR OF SCIENCE IN COMPUTER SCIENCE

RCCS 108: COMPUTER ORGANIZATION & ASSEMBLY.

DATE: 4th/ April /2016. TIME: 2 HOURS

GENERAL INSTRUCTIONS:

Students are NOT permitted to write on the examination paper during reading time.

This is a closed book examination. Text book/Reference books/notes are not permitted.

SPECIAL INSTRUCTIONS:

This examination paper consists Questions in Section A followed by section B.

Answer **Question 1 and any Other Two** questions.

QUESTIONS in ALL Sections should be answered in answer booklet(s).

1. **PLEASE start the answer to EACH question on a NEW PAGE. You will lose 5 MARKS if this is not done.**
2. **Keep your phone(s) switched off at the front of the examination room and NOT on your person.**
3. **Keep ALL bags and caps at the front of the examination room and DO NOT refer to ANY unauthorized material before or during the course of the examination.**
4. **ALWAYS show your working.**
5. **Marks indicated in parenthesis i.e. ( ) will be awarded for clear and logical answers.**
6. **Write your REGISTRATION No. clearly on the answer booklet(s).**
7. **For the Questions, write the number of the question on the answer booklet(s) in the order you answered them.**
8. **Calculator will be required.**
9. **Microprocessor Instruction Set will be provided**

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SECTION A (COMPULSORY)

Question (1) - (30Marks)

a) Define the following terms. **(10 Marks)**

i. S.M.A.R.T.
ii. R.A.I.D.
iii. B.I.O.S.
iv. S.C.I.S.
v. R.I.S.C.
vi. C.I.S.C.
vii. Machine Language.
viii. Macro Instructions.
ix. Micro Instructions.
x. Dynamic Execution

b) Name types of buses found in computers, and hence explain the purpose of each. **(3 Marks)**

c) Describe the purpose of the Assembler, Interpreter, and Compiler. **(3 Marks)**

d) With respect to Intel's Instruction Set Architecture (ISA), list five categories of instructions, and give example of each classification. **(10 Marks)**

e) Describe in details, the ***Fetch Execute cycle*** of a microprocessor. **(4 Marks)**

(You can use a timing diagram in describing, if necessary)

SECTION B (Answer Any Two Questions)

Question (2) - (20Marks)

a) Differentiate between the high and low level programming languages; hence give two examples in each. **(4 Marks)**

b) With reference to Intel-8085 microprocessor and using a suitable flow-chat, Write a program to add three numbers stored in the memory locations 3000_{Hex}, 3001_{Hex} & 3002_{Hex} respectfully, and then store the result of the operation in the memory location 3010_{Hex}. Hence Output the binary result Through Port $A8_{Hex}$.

(The instruction set for Intel 8085 will be provided at the back page). **(10 Marks)**

c) Highlight main differences between the Harvard and the Von Neumann architectures of computers CPUs. **(6 Marks)**

Question (3) - (20Marks)

a) With respect to Intel 8085 microprocessor, explain the functions of the following assembly instructions. **(10 Marks)**

i. **ADC** *B*
ii. **STA** $FFFF_{hex}$
iii. **MOV** *M, C*
iv. **DAA**
v. **PUSH** *B*
vi. **NOP**
vii. **CALL** $FAAA_{hex}$
viii. **JNC** 2034_{hex}
ix. **OUT** $F8_{hex}$
x. **CMC**

b) State five addressing modes for the Intel x86 architecture, and hence give example of an instruction in each case. **(10 Marks)**

Question (4) - (20Marks)

a) Using 4-chips of (16K X 8) and a suitable decoder, design a memory array of (64K x 8). Clearly show the data buses, address buses, and indicate the memory chips and their addresses range. **(10 Marks)**

b) Name five types of networks and indicate the main communication medium used in each. **(5 Marks)**

c) Explain the meaning of the following terms as used in computer science. **(5 Marks)**

i. Polling.
ii. Pipelining.
iii. Hyper threading.
iv. Multiprocessing.
v. Parallel computing.

Question (5) - (20Marks)

a) Microprocessors use registers to temporarily store data while processing. **(5 Marks)** Name the common registers used and specify how they are utilised.

b) Describe the following types of Random Access Memories. **(3 Marks)**

i. SRAM.
ii. SDRAM.
iii. DDR-SDRAM

c) A computer system has 32 bits address buses, 32 bits data buses, and 8 bit control buses.

i. What is the maximum size of the word can it handle? **(1 Marks)**
ii. What is the maximum size of RAM can the system address? **(1 Marks)**

d) The program below test RAM by writing '1' (one) and reading it back and later writing '0' (Zero) and reading it back. It is meant to test the RAM addresses 4000H to 40FFH. In case of any error, it is indicated by lighting an LED diode connected to LSB of port 10H, by out-putting 01H to the port.
Assemble the program to determine how much of the RAM the program will require.
(The instruction set for Intel 8085 will be provided at the back page). **(10 Marks)**

Source Program:

```
        LXI H, 4000hex          : Initialize memory pointer
BACK0:  MVI M, FFhex            : Writing '1' into RAM
        MOV A, M                : Reading data from RAM
        CPI FFH                 : Check for ERROR
        JNZ ERROR               : If yes go to ERROR
        INX H                   : Increment memory pointer
        MOV A, H
        CPI 00hex               : Check for last check
        JNZ BACK0               : If not last, repeat
        LXI H, 4000hex          : Initialize memory pointer
BACK1:  MVI M, OOH              : Writing '0' into RAM
        MOV A, M                : Reading data from RAM
        CPI 00hex               : Check for ERROR
        INX H                   : Increment memory pointer
        MOV A, H
        CPI 00hex               : Check for last check
        JNZ BACK1               : If not last, repeat
ERROR:  LDI A, 01 hex           : load error output value
        OUT 10 hex              : output error value
        HLT                     : Stop Execution
```

8080/85 CPU INSTRUCTIONS IN OPERATION CODE SEQUENCE

OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC
00	NOP	2B	DCX H	56	MOV D,M
01	LXI B,D16	2C	INR L	57	MOV D,A
02	STAX B	2D	DCR L	58	MOV E,B
03	INX B	2E	MVI L,D8	59	MOV E,C
04	INR B	2F	CMA	5A	MOV E,D
05	DCR B	30	SIM	5B	MOV E,L
06	MVI B,D8	31	LXI SPD16	5C	MOV E,H
07	RLC	32	STA Adr	5D	MOV E,L
08	—	33	INX SP	5E	MOV E,M
09	DAD B	34	INR M	5F	MOV E,A
0A	LDAX B	35	DCR M	60	MOV H,B
0B	DCX B	36	MVI M,D8	61	MOV H,C
0C	INR C	37	STC	62	MOV H,D
0D	DCR C	38	—	63	MOV H,E
0E	MVI C,D8	39	DAD SP	64	MOV H,H
0F	RRC	3A	LDA Adr	65	MOV H,L
10		3B	DCX SP	66	MOV H,M
11	LXI D,D16	3C	INR A	67	MOV H,A
12	STAX D	3D	DCR A	68	MOV L,B
13	INX D	3E	MVI A,D8	69	MOV L,C
14	INR D	3F	CMC	6A	MOV L,D
15	DCR D	40	MOV B,B	6B	MOV L,E
16	MVI D,D8	41	MOV B,C	6C	MOV L,H
17	RAL	42	MOV B,D	6D	MOV L,L
18		43	MOV B,E	6E	MOV L,M
19	DAD D	44	MOV B,H	6F	MOV L,A
1A	LDAX D	45	MOV B,L	70	MOV M,B
1B	DCX D	46	MOV B,M	71	MOV M,C
1C	INR E	47	MOV B,A	72	MOV M,D
1D	DRC E	48	MOV C,B	73	MOV M,E
1E	MVI E,D8	49	MOV C,C	74	MOV M,H
1F	RAR	4A	MOV C,D	75	MOV M,L
20	RIM	4B	MOV C,E	76	HLT
21	LXI H,D16	4C	MOV C,H	77	MOV M,A
22	SHLD Adr	4D	MOV C,L	78	MOV A,B
23	INX H	4E	MOV C,M	79	MOV A,C
24	INR H	4F	MOV C,A	7A	MOV A,D
25	DCR H	50	MOV D,B	7B	MOV A,E
26	MVI H,D8	51	MOV D,C	7C	MOV A,H
27	DAA	52	MOV D,D	7D	MOV A,L
28	-	53	MOV D,E	7E	MOV A,M
29	DAD H	54	MOV D,H	7F	MOV A,A
2A	LHLD Adr	55	MOV D,L	80	ADD B

OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC
81	ADD C	AC	XRA H	D7	RST 2
82	ADD D	AD	XRA L	D8	RC
83	ADD E	AE	XRA M	D9	
84	ADD H	AF	XRA A	DA	JC Adr
85	ADD L	B0	ORA B	DB	IN D8
86	ADD M	B1	ORA C	DC	CC Adr
87	ADD A	B2	ORA D	DD	—
88	ADC B	B3	ORA E	DE	SBI D8
89	ADC C	B4	ORA H	DF	RST 3
8A	ADC D	B5	ORA L	E0	RPO
8B	ADC E	B6	ORA M	E1	POP H
8C	ADC H	B7	ORA A	E2	JPO Adr
8D	ADC L	B8	CMP B	E3	XTHL
8E	ADC M	B9	CMP C	E4	CPO Adr
8F	ADC A	BA	CMP D	E5	PUSH H
8G	SUB B	BB	CMP E	E6	ANI D8
91	SUB C	BC	CMP H	E7	RST 4
92	SUB D	BD	CMP L	E8	RPE
93	SUB L	BE	CMP M	E9	PCHL
94	SUB H	BF	CMP A	EA	JPE Adr
95	SUB L	C0	RNZ	EB	XCHG
96	SUB M	C1	POP B	EC	CPE Adr
97	SUB A	C2	JNZ Adr	ED	
98	SBB B	C3	JMP Adr	EE	XRI D8
99	SBB C	C4	CNZ Adr	EF	RST 5
9A	SBB D	C5	PUSH B	F0	RP
9B	SBB E	C6	ADI D8	F1	POP PSW
9C	SBB H	C7	RST 0	F2	JP Adr
9D	SBB L	C8	RZ	F3	DI
9E	SBB M	C9	RET Adr	F4	CP Adr
9F	SBB A	CA	JZ	F5	PUSH PSW
A0	ANA B	CB	-	F6	ORI D8
A1	ANA C	CC	CZ Adr	F7	RST 6
A2	ANA D	CD	CALL Adr	F8	RM
A3	ANA E	CE	ACI D8	F9	SPHL
A4	ANA H	CF	RST 1	FA	JM Adr
A5	ANA L	D0	RNC	FB	EI
A6	ANA M	D1	POP D	FC	CM Adr
A7	ANA A	D2	JNC Adr	FD	---
A8	XRA B	D3	OUT D8	FE	CPI D8
A9	XRA C	D4	CNC Adr	FF	RST 7
AA	XRA D	D5	PUSH D		
AB	XRA E	D6	SUI D8		

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity.

D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity

Adr = 16-bit address