UNIVERSITY EXAMINATIONS

EXAMINATION FOR SEPTEMBER/DECEMBER 2019/2020 FOR BACHELOR OF SCIENCE IN COMPUTER SCIENCE

RCCS 108: COMPUTER ORGANIZATION & ASSEMBLY LANGAUGE.

DATE: 19TH DECEMBER 2019 **TIME: 2 HOURS**

GENERAL INSTRUCTIONS:

Students are NOT permitted to write on the examination paper during examination time.

This is a closed book examination. Text book/Reference books/notes are not permitted.

SPECIAL INSTRUCTIONS:

This examination paper consists Questions in Section A followed by section B.

Answer **Question 1 and any Other Two** questions.

QUESTIONS in ALL Sections should be answered in answer booklet(s).

1. **PLEASE start the answer to EACH question on a NEW PAGE.**
2. **Keep your phone(s) switched off at the front of the examination room.**
3. **Keep ALL bags and caps at the front of the examination room and DO NOT refer to ANY unauthorized material before or during the course of the examination.**
4. **ALWAYS show your working.**
5. **Marks indicated in parenthesis i.e. ( ) will be awarded for clear and logical answers.**
6. **Write your REGISTRATION No. clearly on the answer booklet(s).**
7. **For the Questions, write the number of the question on the answer booklet(s) in the order you answered them.**
8. **Calculator will be required, DO NOT use your PHONE as a CALCULATOR.**
9. **YOU are ONLY ALLOWED to leave the exam room 30minutes to the end of the Exam.**
10. **DO NOT write on the QUESTION PAPER. Use the back of your BOOKLET for any calculations or rough work.**
11. **Intel 8085 Microprocessor Instruction Set provided at back pages.**

SECTION A (COMPULSORY)

Question (1) - (30Marks)

a) What is the purpose of following hardware in computers systems? **(6 Marks)**

i. FSB.
ii. SSD.
iii. DMAC.
iv. North Bridge.
v. South Bridge.

b) What is the difference between RAM and Cache? **(4 Marks)**

c) With respect to computer memory, **state** and **describe THREE** types of ROM and **THREE** types of RAM. **(6 Marks)**

d) Outline and explain differences between RISC and CISC architectures. **(6 Marks)**

e) A computer system has 16 bits data buses, 32 bits address buses, and 8 bit control buses.

i. What is the maximum size of the word can it handle? **(1 Marks)**
ii. What is the maximum size of RAM the system can address? **(2 Marks)**

f) What are the major differences between High Level languages and Low Level languages? **(5 Marks)**

SECTION B (Answer Any Two Questions)

Question (2) - (20Marks)

a) Define the following terminologies as used in computing. **(8 Marks)**

i. BIOS.
ii. R.I.S.C.
iii. C.I.S.C.
iv. Pipelining.
v. Multiprocessing.
vi. Hyper threading.
vii. Parallel computing.
viii. Dynamic Execution.

b) With respect processors clock frequency and parallel processing, discus how speed of processing could be affected and the advantages and disadvantages of each. **(4 Marks)**

c) Explain the purpose of the following Intel 8085 Processor Instructions. **(6 Marks)**

i. **HLT**
ii. **NOP**
iii. **INX** *H*
iv. **OUT** $F8_h$
v. **JNZ** 2034_h
vi. **STA** *4000H*

d) What is the purpose of the Assembler? **(2 Marks)**

Question (3) - (20Marks)

a) Describe in ***DETAILS***, the ***FETCH EXECUTE CYCLE*** of a microprocessor during the instruction execution. **(7 Marks)**

b) State and explain the purpose of any **FIVE** major types of registers likely to be found in typical microprocessors. **(10 Marks)**

c) Explain how the direct memory access controller would improve computation performance in a computer. **(3 Marks)**

Question (4) - (20Marks)

a) With reference to Intel-8085 microprocessor, write a program to multiply two numbers stored in the memory locations ABC0 $_{Hex}$ & ABC1 $_{Hex}$ respectfully, and then store the result of the operation in the memory location ABCD $_{Hex}$. **(8 Marks)**

b) Considering the flag register of the Intel 8085 microprocessor, describe the operation of the bit components shown below. **(5 Marks)**

S	Z	X	AC	X	P	X	CY

c) With respect to computer architectures, explain main differences between the Harvard and the Von Neumann architectures of computers. **(3 Marks)**

d) Name **FOUR** categories/classifications of instructions in assembly language. **(4 Marks)**

Question (5) - (20Marks)

a) Assuming that the assembly language program below was executed in an 8085 microprocessor based system. What will be the contents of registers (A, B, C, D, E, H and L), after executing the instructions? (Express results in hexadecimal format). Assume that the registers had the following data initially. **(7 Marks)**

Registers	Reg A	Reg B	Reg C	Reg D	Reg E	Reg H	Reg L
Data	FF_{hex}	06_{hex}	04_{hex}	AB_{hex}	CD_{hex}	$F3_{hex}$	$8E_{hex}$

Instruction	Comments
XRA A	
MVI B, F7 $_{Hex}$	
MOV D,A	
MOV C,A	
ADC B	
INX D	
XCHG	

b) Given 8-chips of (16K X 8) and a (3 to 8) decoder, design a memory module for the Intel 8085 based system, showing the data & address buses clearly. **(8 Marks)**

c) Assemble the assembly language program below (next page), hence determine the amount of memory required to run the code. **(5 Marks)**

Assembly Language Source Code Program:

```
LXI H, 2000hex      //- Comments….
MOV B, M            //
INX L               //
MOV C, M            //
XOR A               //
ADC B               //
STA 4000hex         //
OUT 80 hex          //
HLT                 //
```

INTEL 8085 MICROPROCESSOR INSTRUCTION SET

Hex	mnemonic	Hex	mnemonic	Hex	mnemonic	Hex	mnemonic
CE	ACI 8-Bit	3F	CMC	2B	DCX H	01	LXI B,16-Bit
8F	ADC A	BF	CMP A	3B	DCX SP	11	LXI D,16-Bit
88	ADC B	B8	CMP B	F3	DI	21	LXI H,16-Bit
89	ADC C	B9	CMP C	FB	EI	31	LXI SP,16-Bit
8A	ADC D	BA	CMP D	76	HLT	7F	MOV A A
8B	ADC E	BB	CMP E	DB	IN 8-Bit	78	MOV A B
8C	ADC H	BC	CMP H	3C	INR A	79	MOV A C
8D	ADC L	BD	CMP	04	INR B	7A	MOV A D
8E	ADC M	BE	CMP M	0C	INR C	7B	MOV A E
87	ADD A	D4	CNC 16-Bit	14	INR D	7C	MOV A H
80	ADD B	C4	CNZ 16-Bit	1C	INR E	7D	MOV A L
81	ADD C	F4	CP 16-Bit	24	INR H	7E	MOV A M
82	ADD D	EC	CPE 16-Bit	2C	INR L	47	MOV B A
83	ADD E	FE	CPI 8-Bit	34	INR M	40	MOV B B
84	ADD H	E4	CPO 16-Bit	03	INX B	41	MOV B C
85	ADD L	CC	CZ 16-Bit	13	INX D	42	MOV B D
86	ADD M	27	DAA	23	INX H	43	MOV B E
C6	ADI 8-Bit	09	DAD B	33	INX SP	44	MOV B H
A7	ANA A	19	DAD D	DA	JC 16-Bit	45	MOV B L
A0	ANA B	29	DAD H	FA	JM 16-Bit	46	MOV B M
A1	ANA C	39	DAD SP	C3	JMP 16-Bit	4F	MOV C A
A2	ANA D	3D	DCR A	D2	JNC 16-Bit	48	MOV C B
A3	ANA E	05	DCR B	C2	JNC 16-Bit	49	MOV C C
A4	ANA H	0D	DCR C	F2	JP 16-Bit	4A	MOV C D
A5	ANA L	15	DCR D	EA	JPE 16-Bit	4B	MOV C E
A6	ANA M	1D	DCR E	E2	JPO 16-Bit	4C	MOV C H
E6	ANA 8-Bit	25	DCR H	CA	JZ 16-Bit	4D	MOV C L
CD	CALL 16-Bit	2D	DCR L	3A	LDA 16-Bit	4E	MOV C M
DC	CC 16-Bit	35	DCR M	0A	LDAX B	57	MOV D A
FC	CM 16-Bit	0B	DCX B	1A	LDAX D	50	MOV D B
2F	CMA	1B	DCX D	2A	LHLD 16-Bit	51	MOV D C

Hex	mnemonic	Hex	mnemonic	Hex	mnemonic	Hex	mnemonic
52	MOV D D	71	MOV M C	E5	PUSH H	9E	SBB M
53	MOV D E	72	MOV M D	F5	PUSH PSW	DE	SBI 8-Bit
54	MOV D H	73	MOV M E	17	RAL	22	SHLD 16-Bit
55	MOV D L	74	MOV M H	1F	RAR	30	SIM
56	MOV D M	75	MOV M L	D8	RC	F9	SPHL
5F	MOV E A	3E	MVI A 8-Bit	C9	RET	32	STA 16-Bit
58	MOV E B	06	MVI B 8-Bit	20	RIM	02	STAX B
59	MOV E C	OE	MVI C 8-Bit	07	RLC	12	STAX D
5A	MOV E D	16	MVI D 8-Bit	F8	RM	37	STC
5B	MOV E E	1E	MOV E 8-Bit	D0	RNC	97	SUB A
5C	MOV E H	26	MVI H 8-Bit	C0	RNC	90	SUB B
5D	MOV E L	2E	MVI L 8-Bit	F0	RP	91	SUB C
5E	MOV E M	36	MVI M 8-Bit	E8	RPE	92	SUB D
67	MOV H A	00	NOP	E0	RPO	93	SUB E
60	MOV H B	B7	ORA A	0F	RRC	94	SUB H
61	MOV H C	B0	ORA B	C7	RST 0	95	SUB L
62	MOV H D	B1	ORA C	CF	RST 1	96	SUB M
63	MOV H E	B2	ORA D	D7	RST 2	D6	SUI 16-Bit
64	MOV H H	B3	ORA E	DF	RST 3	EB	XCHG
65	MOV H L	B4	ORA H	E7	RST 4	AF	XRA A
66	MOV H M	B5	ORA L	EF	RST 5	A8	XRA B
6F	MOV L A	B6	ORA M	F7	RST 6	A9	XRA C
68	MOV L B	F6	ORI 8-Bit	FF	RST 7	AA	XRA D
69	MOV L C	D3	OUT 8-Bit	C8	RZ	AB	XRA E
6A	MOV L D	E9	PCHL	9F	SBB A	AC	XRA H
6B	MOV L E	C1	POP B	98	SBB B	AD	XRA L
6C	MOV L H	D1	POP D	99	SBB C	AE	XRA M
6D	MOV L L	E1	POP H	9A	SBB D	EE	XRI 8-Bit
6E	MOV L M	F1	POP PSW	9B	SBB E	E3	XTHL
77	MOV M A	C5	PUSH B	9C	SBB H		
70	MOV M B	D5	PUSH D	9D	SBB L		